

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of fabricating a memory cell, said method comprising the steps of:

forming a conductive layer in a trench of an insulating layer;

forming a first dielectric layer having a top surface over said conductive layer and said insulating layer;

forming an opening in said first dielectric layer over said conductive layer;

forming a first magnetic layer within said opening and over said first dielectric layer;

forming a nonmagnetic layer over said first magnetic layer;

forming a second magnetic layer over said nonmagnetic layer;

forming a second dielectric layer over said second magnetic layer; and

planarizing said first magnetic layer, nonmagnetic layer, second magnetic layer, and said second dielectric layer down to said top surface to form said memory cell.
2. The method of claim 1 further comprising removing any unwanted corners from said cell formed from said planarization step.
3. The method of claim 2 wherein said removing is performed by low temperature furnace oxidation.

4. The method of claim 2 wherein said removing is performed by wet chemical oxidation.
5. The method of claim 1 further comprising etching said first and second dielectric layers.
6. The method of claim 1 wherein said opening is a trench.
7. The method of claim 1 wherein said opening is surrounded by said first dielectric layer.
8. The method of claim 1 wherein said step of planarizing is performed by chemical mechanical polishing.
9. The method of claim 1 wherein said first dielectric layer is formed to a thickness at least greater than that of said cell.
10. The method of claim 1 wherein said second magnetic layer is a sense layer.
11. The method of claim 10 wherein said sense layer is formed of plurality of layers to produce a ferromagnetic sense layer.
12. The method of claim 1 wherein said first magnetic layer is a pinned layer.
13. The method of claim 12 wherein said pinned layer is formed of a plurality of layers to produce a ferromagnetic pinned layer.

14. The method of claim 1 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO₂, Si₃N₄ and polyimide.
15. The method of claim 1 wherein said nonmagnetic layer is aluminum oxide.
16. A method of fabricating a memory cell, said method comprising the steps of:
- forming a conductive layer in a first insulating layer;
 - forming a second insulating layer over said conductive layer and said first insulating layer;
 - forming an opening in said second insulating layer over said conductive layer;
 - forming a pinned layer within said opening;
 - forming a nonmagnetic layer within said opening and over said pinned layer; and
 - forming a sense layer within said opening and over said nonmagnetic layer.
17. The method of claim 16 further comprising removing any unwanted corners from said cell formed from said planarization step.
18. The method of claim 17 wherein said removing is performed by low temperature furnace oxidation.
19. The method of claim 17 wherein said removing is performed by wet chemical oxidation.

20. The method of claim 16 further comprising etching said first and second dielectric layers.
21. The method of claim 16 wherein said opening is a trench.
22. The method of claim 16 wherein said opening is surrounded by said second insulating layer.
23. The method of claim 16 wherein said step of planarizing is performed by chemical mechanical polishing.
24. The method of claim 16 wherein said second insulating layer is formed to a thickness at least greater than that of said cell.
25. The method of claim 16 wherein said sense layer is formed of plurality of layers to produce a ferromagnetic sense layer.
26. The method of claim 16 wherein said pinned layer is formed of a plurality of layers to produce a ferromagnetic pinned layer.
27. The method of claim 16 wherein said first insulating layer is selected from the group consisting of BPSG, SiO, SiO₂, Si₃N₄ and polyimide.
28. The method of claim 16 wherein said nonmagnetic layer is aluminum oxide.